What Is Claimed Is:

1. A microcontroller comprising:

a CPU;

a bus controller;

an instruction address bus and an instruction code bus, of a first bit number, which connect said CPU and bus controller; and

a debug support unit, which is connected to said instruction address bus and instruction code bus,

wherein said debug support unit is connected to an external in-circuit emulator via a tool bus whose bit number is smaller than said first bit number and via a bus status signal line which reports on the status of the tool bus; and

wherein said debug support unit comprises:

a parallel to serial conversion circuit, which performs parallel to serial conversion of an instruction address;

a status information generation circuit, which generates a status information signal, which contains branch information and an instruction fetch request, in response to a branch signal and instruction fetch request signal received from said CPU;

a status output circuit, which outputs an instruction address output signal to said bus status signal line in response to the status information signal; and

a data output circuit, which, in response to said status information signal, when said branch information contains a branch, outputs said converted instruction address in series to said tool bus, and when the branch information contains no branch, outputs a branchless signal to said tool bus.

2. The microcontroller according to claim 1, wherein said data-output circuit outputs said converted instruction address in series to said tool bus in a plurality of cycles when said branch information contains a branch, and outputs said branchless signal to said tool bus in a single cycle when the branch information contains no branch.

3. The microcontroller according to claim 1, wherein, after said debug support unit has performed an address output which corresponds to said instruction fetch request, the debug support unit outputs a data receive signal, over a period of a predetermined plurality of cycles, to said bus status signal line, and thus receives instruction code, which corresponds to said instruction fetch request, in series from said in-circuit emulator.

4. The microcontroller according to claim 1, wherein, when said debug support unit receives the instruction fetch request from said CPU, the debug support unit issues a wait signal to said CPU, and when instruction code, which corresponds to the instruction fetch request, is sent to said CPU in response,

the debug support unit cancels said wait signal.

5. The microcontroller according to claim 1, wherein, in a case in which the instruction fetch request and a data access request have been received from said CPU, said debug support unit processes said data access request preferentially.

6. A microcontroller comprising:

a CPU;

a bus controller;

an instruction address bus and an instruction code bus, of a first bit number, which connect said CPU and bus controller; and

a debug support unit, which is connected to said instruction address bus and instruction code bus,

wherein said debug support unit is connected to an external in-circuit emulator via a tool bus whose bit number is smaller than said first bit number and via a bus status signal line which reports on the status of this tool bus;

wherein said debug support unit comprises:

a parallel to serial conversion circuit, which performs parallel to serial conversion of an instruction address;

a status information generation circuit, which generates a status information signal, which contains branch information and an instruction fetch request, in response to a branch signal and instruction fetch request signal received from said CPU;

a status output circuit, which outputs an instruction address output signal to said bus status signal line in response to said status information signal; and

a data output circuit, which, in response to said status information signal, outputs said converted instruction address in series to said tool bus, and

wherein, when said status information generation circuit finishes receiving instruction code which corresponds to a current instruction fetch request before receiving a next instruction fetch request, the status information generation circuit generates a prefetch status information signal for an instruction-prefetch request with an instruction address which succeeds the instruction address of the current instruction fetch request.

7. The microcontroller according to claim 6, wherein, when said status information generation circuit, following initiation of said instruction-prefetch request, receives the instruction fetch request from said CPU and a branch signal which contains a branch, control of said instruction-prefetch request is canceled.

8. The microcontroller according to claim 6, wherein, in response to said prefetch status information signal, said data output circuit outputs a branchless signal, in place of an instruction address, to said tool bus.

9. The microcontroller according to claim 6, wherein said status information generation circuit generates said prefetch status information signal when there is space in a buffer for storage of instruction code received from said in-circuit emulator and when said tool bus is not being used.

10. The microcontroller according to claim 6, wherein, when said debug support unit receives the instruction fetch request from said CPU, the debug support unit issues a wait signal to said CPU, and when instruction code, which corresponds to the instruction fetch request, is sent to said CPU in response, the debug support unit cancels said wait signal.

11. A microcontroller comprising:

a CPU;

and a bus controller;

an address bus, of a first bit number, which connects said CPU and bus controller; and

a debug support unit, which is connected to said address bus,

wherein said debug support unit is connected to an external in-circuit emulator via a tool bus whose bit number is smaller than said first bit number and via a bus status signal line which reports on the status of this tool bus; and

wherein said debug support unit comprises:

an encoder, which outputs an encoded address which includes an effective address contained in an address and an

effective digit number signal for the effective address;

a parallel to serial conversion circuit which performs parallel to serial conversion of said encoded address;

a status information generation circuit, which, in a period of the number of cycles corresponding to said effective digit number, generates a status information signal which contains an instruction fetch request or data access request, in response to an instruction fetch request signal or data access request signal, respectively received from said CPU;

a status output circuit, which outputs an address output signal to said bus status signal line in response to said status information signal; and

a data output circuit, which outputs said encoded address to said tool bus in series in response to said status information signal.

12. The microcontroller according to claim 11, wherein said address bus has an instruction address bus and a data address bus, and said encoder encodes an address which is input via said instruction address bus or data address bus.

13. A microcontroller comprising:

a CPU;

a bus controller;

an instruction address bus, of a first bit number, which connects said CPU and bus controller and transfers an instruction address in parallel; and

a debug support unit, which is connected to said instruction address bus,

wherein said debug support unit is connected to an external in-circuit emulator via a tool bus whose bit number is smaller than said first bit number and via a bus status signal line which reports on the status of the tool bus; and

wherein, in a case in which an instruction fetch request received from said CPU is an instruction with a branch, said debug support unit performs parallel to serial conversion of the instruction address, and then outputs the converted instruction address to said tool bus in series, and, in a case in which said instruction fetch request is a branchless instruction, outputs a branchless signal to said tool bus.

14. A microcontroller comprising:

a CPU;

a bus controller;

an instruction address bus and instruction code bus, of a first bit number, which connects said CPU and bus controller and transfers an instruction address in parallel; and

a debug support unit, which is connected to said instruction address bus and instruction code bus;

wherein said debug support unit is connected to an external in-circuit emulator via a tool bus whose bit number is smaller than said first bit number and via a bus status signal line which reports on the status of the tool bus; and

wherein said debug support unit outputs said

instruction address to said tool bus in series in response to an instruction fetch request signal received from said CPU, and initiates instruction-prefetch control when instruction code, which corresponds to the instruction fetch request, has been received from said in-circuit emulator, before a next instruction fetch request is received.

15. The microcontroller according to claim 14, wherein, if, in the course of said instruction prefetch control, said debug support unit receives an instruction fetch request which contains a branch from said CPU, the debug support unit cancels the instruction prefetch control, and transfers a branch instruction address to said tool bus in series.

16. A microcontroller comprising:

a CPU;

a bus controller;

an address bus, of a first bit number, which connects said CPU and bus controller; and

a debug support unit, which is connected to said address bus,

wherein said debug support unit is connected to an external in-circuit emulator via a tool bus whose bit number is smaller than said first bit number and via a bus status signal line which reports on the status of the tool bus; and

wherein said debug support unit comprises a data output circuit, which generates an encoded address which includes

an effective address contained in an address and an effective digit number signal for the effective address, and which outputs said encoded address to said tool bus in series in response to an instruction fetch request signal or data access request signal received from said CPU.